A5833

BiMOS II 32-Bit Serial Input Latched Driver

Last Time Buy

These parts are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: May 2, 2005

Deadline for receipt of LAST TIME BUY orders: October 28, 2005

Recommended Substitutions:

For new customers or new applications, refer to the <u>A6833</u>.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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BiMOS II 32-BIT SERIAL-INPUT, LATCHED DRIVER

Designed to reduce logic supply current, chip size, and system cost, the UCN5833A/EP integrated circuits offer high-speed operation for thermal printers. These devices can also be used to drive multiplexed LED displays or incandescent lamps within their 125 mA peak output current rating. The combination of bipolar and MOS technologies gives BiMOS II smart power ICs an interface flexibility beyond the reach of standard buffers and power driver circuits.

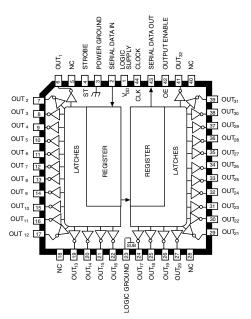
These 32-bit drivers have bipolar open-collector npn Darlington outputs, a CMOS data latch for each of the drivers, a 32-bit CMOS shift register, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor-based systems at data input rates above 3.3 MHz. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high.

The UCN5833A is supplied in a 40-pin dual in-line plastic package with 0.600" (15.24 mm) row spacing. At an ambient temperature of +75°C, all outputs of the DIP-packaged device will sustain 50 mA continuously. For high-density applications, the UCN5833EP is available. This 44-lead plastic chip carrier (quad pack) is intended for surface-mounting on solder lands with 0.050" (1.27 mm) centers. CMOS serial data outputs permit cascading for applications requiring additional drive lines.

FEATURES

- To 3.3 MHz Data Input Rate
- 30 V Minimum Output Breakdown
- Darlington Current-Sink Outputs
- Low-Power CMOS Logic and Latches

UCN5833EP



Dwg. No. A-13,049

ABSOLUTE MAXIMUM RATINGS

at +25°C Free-Air Temperature

Output Voltage, V _{OUT} 30 V
Logic Supply Voltage, V _{DD} 7.0 V
Input Voltage Range,
V_{IN} 0.3 V to V_{DD} + 0.3 V
Continuous Output Current,
I _{OUT} (each output) 125 mA
Package Power Dissipation, P _D
(UCN5833A) 3.5 W*
(UCN5833EP) 2.5 W*
Operating Temperature Range,
T _A 20°C to +85°C
Storage Temperature Range,
$T_S \dots T_{S-1} - 55^{\circ}C$ to +150°C

* Derate linearly to 0 W at +150°C.

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

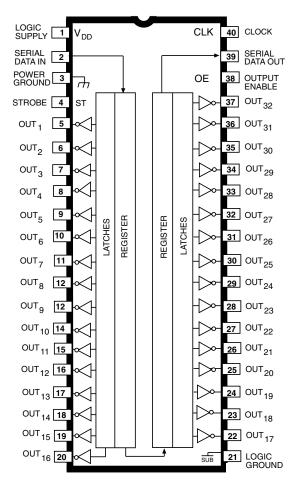
Always order by complete part number:

Part Number	Package
UCN5833A	40-Pin DIP
UCN5833EP	44-Lead PLCC

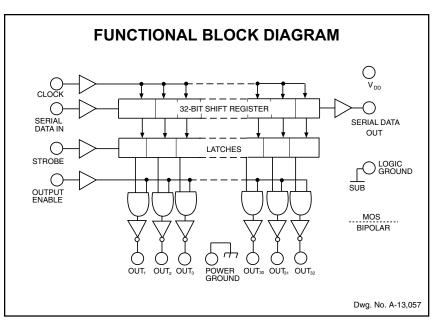


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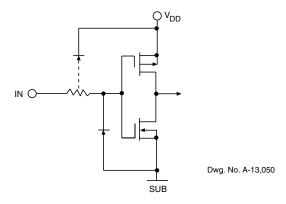
UCN5833A



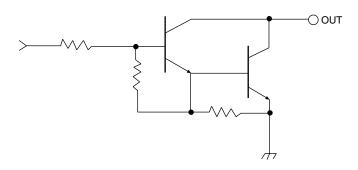
Dwg. No. A-13,048



TYPICAL INPUT CIRCUIT



TYPICAL OUTPUT DRIVER



Dwg. No. A-13,051



ELECTRICAL CHARACTERISTICS at T $_{\rm A}$ = +25 $^{\circ}$ C, V $_{\rm DD}$ = 5 V (unless otherwise noted).

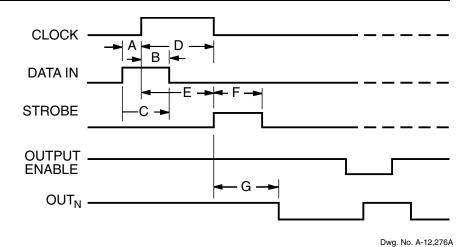
			Limits							
Characteristic	Symbol	Test Conditions	Min.	Max.	Units					
Output Leakage Current	I _{CEX}	V _{OUT} = 30 V, T _A = 70°C	_	10	μΑ					
Collector-Emitter	V _{CE(SAT)}	I _{OUT} = 50 mA	_	1.2	V					
Saturation Voltage		I _{OUT} = 100 mA	_	1.7	V					
Input Voltage	V _{IN(1)}		3.5	5.3	V					
	V _{IN(0)}		-0.3	+0.8	V					
Input Current	I _{IN(1)}	V _{IN} = 5.0 V	_	1.0	μΑ					
	I _{IN(0)}	V _{IN} = 0 V	_	-1.0	μΑ					
Serial Output Voltage	V _{OUT(1)}	I _{OUT} = -200 μA	4.5	_	V					
	V _{OUT(0)}	I _{OUT} = 200 μA	_	0.3	V					
Supply Current	I _{DD}	One output ON, I _{OUT} = 100 mA	_	1.0	mA					
		All outputs OFF	_	50	μА					
Output Rise Time	t _r	I _{OUT} = 100 mA, 10% to 90%	_	500	ns					
Output Fall Time	t _f	I _{OUT} = 100 mA, 90% to 10%	_	500	ns					

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TRUTH TABLE

Serial			hift	Regi	ister	Cont	ents	Serial			Lat	ch C	Cont	ents		Output						
Data Input	Clock Input		l ₂	l ₃		I _{N-1}	I _N	Data Output	Strobe Input		l ₂	l ₃		I _{N-1}	I _N	Enable Input	l ₁	l ₂	₂ I ₃		I _{N-1}	I _N
Н		Н	R ₁	R ₂		R _{N-2}	R _{N-1}	R _{N-1}														
L	7	L	R ₁	R ₂		R _{N-2}	R _{N-1}	R _{N-1}														
Х	7	R ₁	R ₂	R ₃		R _{N-1}	R _N	R _N														
		Х	Х	Χ		Х	Х	Х	L	R ₁	R ₂	R ₃		R _{N-1}	R _N							
		P ₁	P_2	P_3		P _{N-1}	P_N	P _N	Н	P_1	P_2	P_3		P _{N-1}	P_N	Н	P ₁	Р	P ₂ P ₃	3	P _{N-1}	P_N
										Х	Х	Χ		Х	Х	L	Н	Н	ΙН		Н	Н

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State



TIMING CONDITIONS

 $(V_{DD} = 5.0 \text{ V}, \text{Logic Levels are } V_{DD} \text{ and Ground})$

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 ns
C. Minimum Data Pulse Width	150 ns
D. Minimum Clock Pulse Width	150 ns
E. Minimum Time Between Clock Activation and Strobe	300 ns
F. Minimum Strobe Pulse Width	100 ns
G. Typical Time Between Strobe Activation and Output Transition	500 ns

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

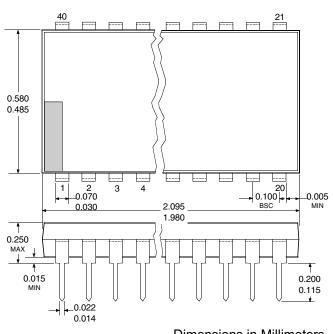
Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

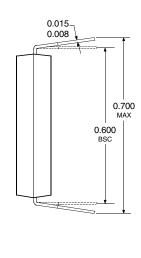
When the OUTPUT ENABLE input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the OUTPUT ENABLE input high, the outputs are controlled by the state of the latches.



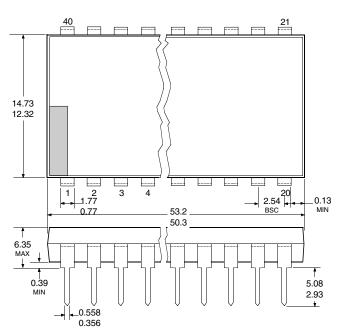
UCN5833A

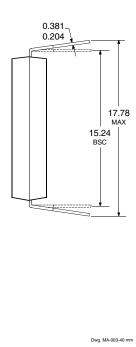
Dimensions in Inches (controlling dimensions)





Dimensions in Millimeters (for reference only)





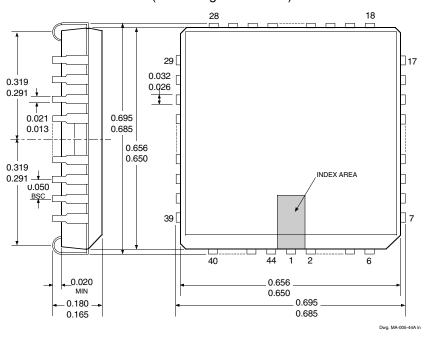
Dwg. MA-003-40 in

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.

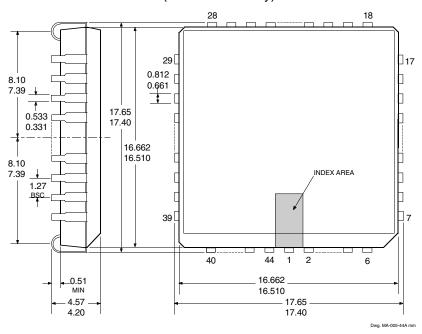
- 2. Lead spacing tolerance is non-cumulative.
- 3. Lead thickness is measured at seating plane or below.

UCN5833EP

Dimensions in Inches (controlling dimensions)



Dimensions in Millimeters (for reference only)



NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.

2. Lead spacing tolerance is non-cumulative.



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The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

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POWER INTERFACE DRIVERS

Function	Output I	Ratings*	Part Number [†]						
SERIAL-INPUT LATCHED DRIVERS									
8-Bit (saturated drivers)	-120 mA	50 V‡	5895						
8-Bit	350 mA	50 V	5821						
8-Bit	350 mA	80 V	5822						
8-Bit	350 mA	50 V‡	5841						
8-Bit	350 mA	80 V‡	5842						
8-Bit (constant-current LED driver)	75 mA	17 V	6275						
8-Bit (DMOS drivers)	250 mA	50 V	6595						
8-Bit (DMOS drivers)	350 mA	50 V‡	6A595						
8-Bit (DMOS drivers)	100 mA	50 V	6B595						
10-Bit (active pull-downs)	-25 mA	60 V	5810-F and 6809/10						
12-Bit (active pull-downs)	-25 mA	60 V	5811 and 6811						
16-Bit (constant-current LED driver)	75 mA	17 V	6276						
20-Bit (active pull-downs)	-25 mA	60 V	5812-F and 6812						
32-Bit (active pull-downs)	-25 mA	60 V	5818-F and 6818						
32-Bit	100 mA	30 V	5833						
32-Bit (saturated drivers)	100 mA	40 V	5832						
PARALLEI	L-INPUT LATCHED	DRIVERS							
4-Bit	350 mA	50 V‡	5800						
8-Bit	-25 mA	60 V	5815						
8-Bit	350 mA	50 V‡	5801						
8-Bit (DMOS drivers)	100 mA	50 V	6B273						
8-Bit (DMOS drivers)	250 mA	50 V	6273						
SPECIAL-PURPOSE DEVICES									
Unipolar Stepper Motor Translator/Driver	1.25 A	50 V‡	5804						
Addressable 8-Bit Decoder/DMOS Driver	250 mA	50 V	6259						
Addressable 8-Bit Decoder/DMOS Driver	350 mA	50 V‡	6A259						
Addressable 8-Bit Decoder/DMOS Driver	100 mA	50 V	6B259						
Addressable 28-Line Decoder/Driver	450 mA	30 V	6817						

^{*} Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits. Negative current is defined as coming out of (sourcing) the output.



[†] Complete part number includes additional characters to indicate operating temperature range and package style.

[‡] Internal transient-suppression diodes included for inductive-load protection.